What is claimed is:

1. A method of forming bit line contact comprising the steps of:

providing a substrate having a plurality of transistors therein, each comprising a gate electrode and doping areas serving as drain and source;

forming a polysilicon spacer on the sidewalls of the gate electrodes;

forming a mask layer to cover a portion of the polysilicon spacer, and removing the unmasked portion of the polysilicon spacer;

removing the mask layer and forming a dielectric layer overlying the surface of the gate electrodes, polysilicon spacers and doping areas; and

using the polysilicon spacer and the substrate as an etch stop, etching a portion of the dielectric layer to form a bit line contact.

2. The method of forming bit line contact as claimed in claim 1, wherein formation of a polysilicon spacer on the sidewalls of the gate electrode further comprises:

forming a conformal polysilicon layer on the surface of the gate electrodes and doping areas; and

anisotropically etching the polysilicon layer, such that the remaining polysilicon layer forms a polysilicon spacer on the sidewalls of the gate electrodes.

3. The method of forming bit line contact as claimed in claim 2, wherein the polysilicon layer is formed by low pressure chemical vapor deposition (LPCVD).

4. The method of forming bit line contact as claimed in claim 2, wherein the polysilicon spacer is etched using magnetic enhanced reactive ion (MERIE), electron cyclotron resonance plasma (ECR), or reactive ion etching (RIE).

5. The method of forming bit line contact as claimed in claim 1, wherein the dielectric layer comprises boro-phosphosilicate glass (BPSG), high density plasma chemical vapor deposition (HDPCVD) oxide, oxygen-containing silicate, or combinations thereof.

6. The method of forming bit line contact as claimed in claim 1, wherein the dielectric layer is formed using low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), atmosphere pressure chemical vapor deposition (APCVD), or second atmosphere pressure chemical vapor deposition(SACVD).

7. The method of forming bit line contact as claimed in claim 1, wherein the gate electrode comprises a cap layer on the top of the gate electrode, and a silicon nitride spacer on the sidewalls of the gate electrode.

8. The method of forming bit line contact as claimed in claim 7, wherein during etching of the unmasked polysilicon spacer, the etching selectivity of the

polysilicon spacer to the cap layer of the gate electrode exceeds 50:1.

9. The method of forming bit line contact as claimed in claim 1, further comprising, before forming the dielectric layer, forming a liner layer on the surface of the gate electrodes, polysilicon spacers, and doping areas.

10. The method of forming bit line contact as claimed in claim 9, wherein the liner layer is silicon nitride.

11. The method of forming bit line contact as claimed in claim 9, wherein the dielectric layer and liner layer are etched using magnetic enhanced reactive ion (MERIE), electron cyclotron resonance plasma (ECR), or reactive ion etching (RIE).

12. A method of forming bit line contact comprising the steps of:

providing a substrate having a plurality of transistors therein, each including a gate electrode and doping areas serving as drain and source;

forming a conformal polysilicon layer on the surface of the gate electrodes and doping areas;

etching the polysilicon layer, such that the polysilicon layer forms a polysilicon spacer on the sidewalls of the gate electrodes;

forming a mask layer on the surface of the gate electrode doping area and a portion of the gate electrode located on both sides of the doping

area; and removing the unmasked portion of the polysilicon spacer by etching;

removing the mask layer and forming a liner layer overlying the surface of the gate electrodes, the polysilicon spacers and the doping areas;

forming a dielectric layer on the liner layer;

using the polysilicon spacer and the doping area as an etch stop; etching a portion of the dielectric layer and the liner layer to form a bit line contact; and

filling a conductive layer into the bit line contact as a bit line contact plug.

13. The method of forming bit line contact as claimed in claim 12, wherein the polysilicon layer is formed by low pressure chemical vapor deposition (LPCVD).

14. The method of forming bit line contact as claimed in claim 12, wherein the polysilicon spacer is etched using magnetic enhanced reactive ion (MERIE), electron cyclotron resonance plasma (ECR) or reactive ion etching (RIE).

15. The method of forming bit line contact as claimed in claim 12, wherein the dielectric layer comprises boro-phosphosilicate glass (BPSG), high density plasma chemical vapor deposition (HDPCVD) oxide, oxygen-containing silicate, or combinations thereof.

16. The method of forming bit line contact as claimed in claim 12, wherein the dielectric layer is formed using low pressure chemical vapor deposition (LPCVD), plasma

enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), atmosphere pressure chemical vapor deposition (APCVD), or second atmosphere pressure chemical vapor deposition(SACVD).

17. The method of forming bit line contact as claimed in claim 12, wherein the gate electrode comprises a cap layer on the top of the gate electrode, and a silicon nitride spacer on the sidewalls of the gate electrode.

18. The method of forming bit line contact as claimed in claim 17, wherein during etching of the unmasked polysilicon spacer, etching selectivity of the polysilicon spacer to the cap layer of the gate electrode exceeds 50:1.

19. The method of forming bit line contact as claimed in claim 12, wherein the liner layer is silicon nitride.

20. The method of forming bit line contact as claimed in claim 12, wherein the dielectric layer and liner layer are etched using magnetic enhanced reactive ion (MERIE), electron cyclotron resonance plasma (ECR), or reactive ion etching (RIE).

21. A method of forming bit line contact comprising the steps of:

providing a substrate having a plurality of transistors therein, each including a gate electrode and doping areas serving as drain and source;

forming a pair of barrier spacers on the opposite sidewalls between gate electrodes;

forming a dielectric layer on the surface of the gate electrodes, barrier spacers and doping areas; and

using the barrier spacer and the substrate as an etch stop, etching a portion of the dielectric layer to form a bit-line contact.

22. The method of forming bit line contact as claimed in claim 21, wherein the barrier spacer comprises materials having barrier, conductivity, or semiconducting properties, or combinations thereof.

23. The method of forming bit line contact as claimed in claim 21, wherein during etching of the portion of the dielectric layer, the etching selectivity of the barrier spacer to the dielectric layer exceeds 50:1.

24. The method of forming bit line contact as claimed in claim 21, wherein the dielectric layer comprises boro-phosphosilicate (BPSG), high density plasma chemical vapor deposition (HDPCVD) oxide, oxygen-containing silicate, or combinations thereof.

25. The method of forming bit line contact as claimed in claim 12, wherein the dielectric layer is formed by low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), atmosphere pressure chemical vapor deposition (APCVD), or second atmosphere pressure chemical vapor deposition(SACVD).

26. The method of forming bit line contact as claimed in claim 21, wherein the gate electrode comprises a cap layer on the top of the gate electrode, and a silicon nitride spacer on the sidewalls of the gate electrode.

27. The method of forming bit line contact as claimed in claim 21, further comprising, before forming the dielectric layer, forming a liner layer on the surface of the gate electrodes, barrier spacers, and doping areas.

28. The method of forming bit line contact as claimed in claim 27, wherein the liner layer is silicon nitride.